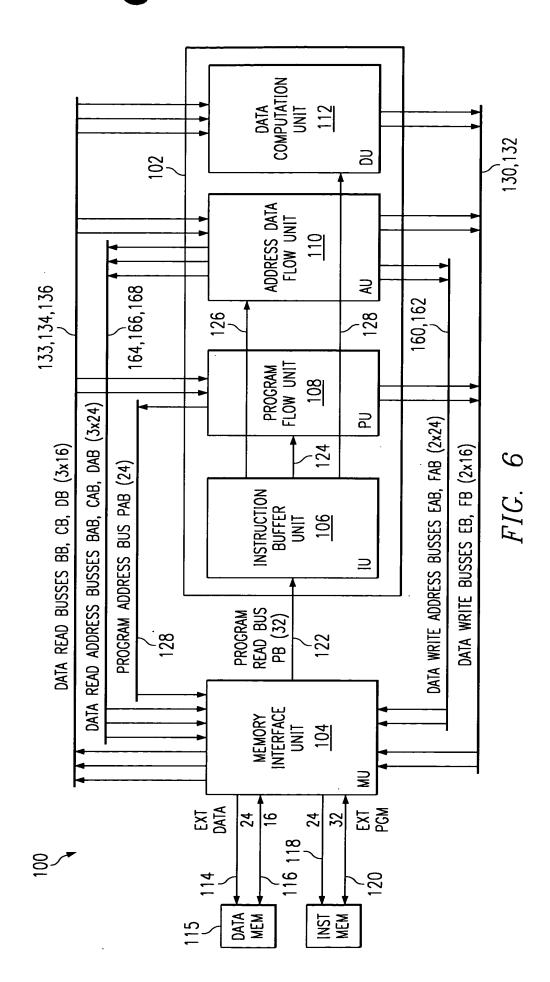


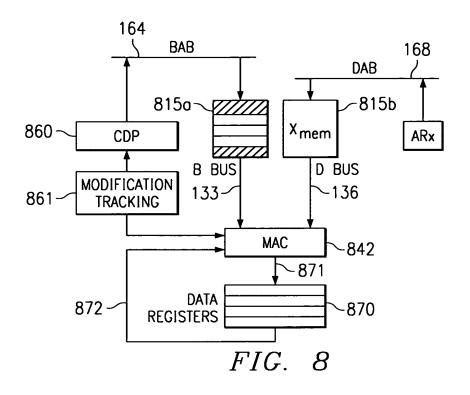
FIG. 4

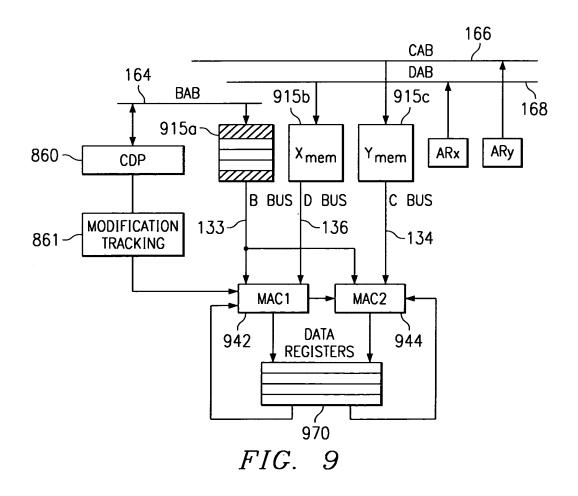
	t ₁	t ₂	tз	t ₄	t ₅	t ₆	t ₇	t ₈	tg	t ₁₀	t ₁₁
	202	204	206	208	210	212	2 2 1 4	1			
302 \INST_1	PF ₁	F ₁	D ₁	AD ₁	AC ₁	R ₁	E ₁				
304 _INST 2		PF ₂	F ₂	D ₂	AD ₂	AC ₂	R ₂	E ₂			
$306 \sim \overline{\text{INST 3}}$	•		PF3	Fz	D3	AD ₃	AC3	R ₃	Eз		
308~INST 4				PF ₄	F ₄	D ₄	AD ₄	AC ₄	R ₄	E4	
310 / INST 5					PF ₅	F ₅	D ₅	AD ₅	AC ₅	R ₅	
312 / INST 6						PF ₆	F ₆	D ₆	^{AD} 6	AC ₆	R ₆
314 / INST 7							PF ₇	F ₇	D ₇	AD ₇	AC ₇
		, =		FI	G.	5					

BYTE ADDRESS (HEX)	PROGRAM MEMORY (ADDRESSING VIA PROGRAM FETCH MECHANISM)	DATA MEMORY (ADDRESSING VIA DATA FETCH MECHANISM)	WORD ADDRESS (HEX) 00 0000 00 0060		
00 0000		MMR			
		MAIN DATA PAGE O	00 0000		
02 0000 02 00C0		MMR	01 0000		
02 0000		MAIN DATA PAGE 1	01 0060		
FE 0000 FE 00C0		MMR	7F 0000		
		MAIN DATA PAGE	7F 0060		
FF FFFF —————		127	7F FFFF		

FIG. 7







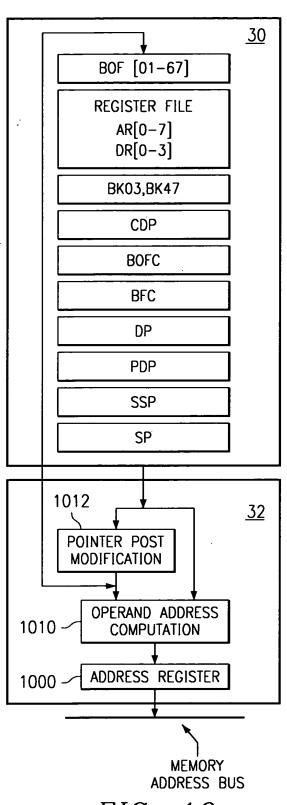
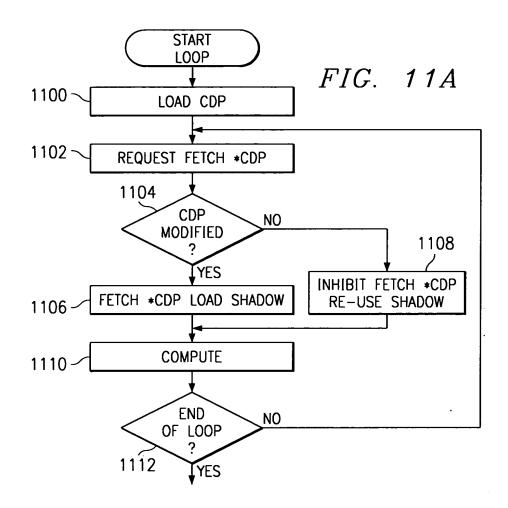
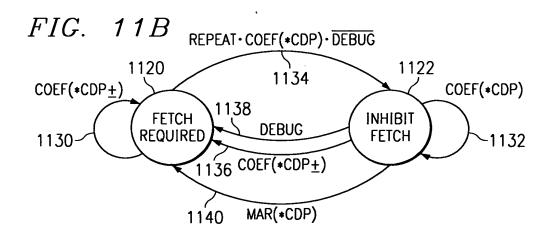


FIG. 10





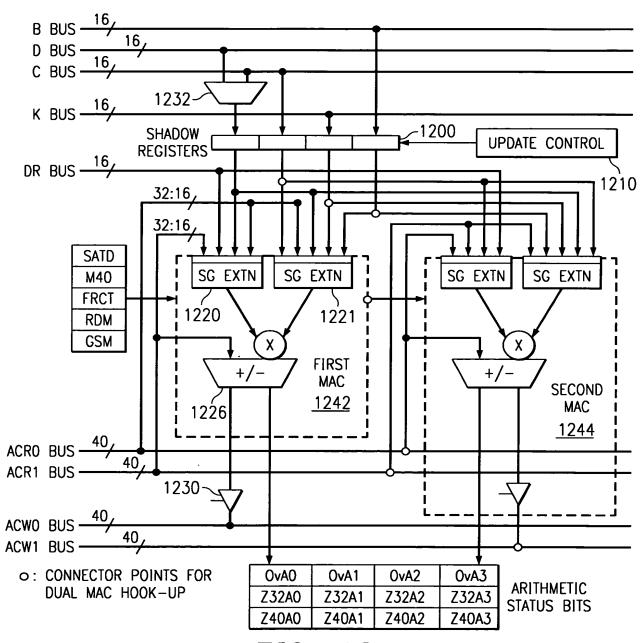


FIG. 12

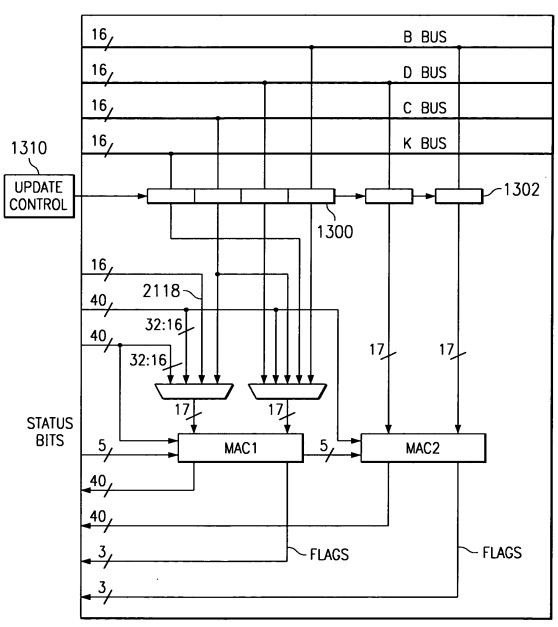


FIG. 13

